REMARKS/ARGUMENTS

Claims 1-42 stand rejected in the outstanding Official Action. Claim 1 has been amended and therefore claims 1-42 remain in this application.

The Examiner's indication of acceptance of the previously submitted formal drawings is very much appreciated. Additionally, the Examiner's confirmation that the objection to the title, objections to claims 15 and 35-39 and the rejections of claims 1 and 22 under §112 are all withdrawn is very much appreciated.

In paragraph 5 of the outstanding Final Rejection, the Examiner requests Applicant to delete the duplicate word "together" from line 9 in claim 1. Applicant offers the above amendment to claim 1 deleting the first word "together."

Entry of the Amendment Pursuant to 37 CFR 1.116

Applicant respectfully requests entry of the above amendment pursuant to the provisions of 37 CFR 1.116 in that the amendment complies with the Examiner's request in eliminating the duplicate word "together." Entering this amendment does not raise any additional issues requiring further consideration or search, does not add new matter to the application, does not additional claims requiring additional search and is believed to place the application in better condition for appeal should an appeal be necessary by eliminating the issue of the typographical error involving the duplicate recitation of the word "together." Pursuant to the provisions under Rule 116, entry is respectfully requested.

Claims 1-42 stand rejected as being anticipated by Applicant's Admitted Prior Art and the details of this rejections are set out in the outstanding Final Rejection in sections 7-29. Inasmuch as these sections 7-29 appear to be identical to sections 8-30 in the previous Official Action

mailed March 7, 2006 (Paper No. 20060218), Applicant's previously filed Amendment of July 7, 2006 is herein incorporated by reference. In addition, the Final Rejection in sections 30-33 includes responses to the Applicant's arguments and Applicant responds below to the points made in those sections.

Notwithstanding the Examiner's quotation from the MPEP §2181, the position of the U.S. PTO does not coincide with the position of the Court of Appeals for the Federal Circuit which is the reviewing authority for the construction of the sixth paragraph of 35 USC §112. It is also recognized in the MPEP that "lack of such language [recitation of "means" or "step"] does not prevent a limitation from being construed as a means-(or step-)plus-function limitation" following the Federal Circuit's decision in *Signtech USA, Ltd. v. Vutek, Inc.* 50 USPQ2d 1372, 1374-5 (Fed. Cir. 1999). An example of such a construction is set out in the MPEP Section 2181, from *Mas-Hamilton Group v. LaGard Inc.*, 48 USPQ2d 1010, 1016 (Fed. Cir. 1998), where the Court held

> 'lever moving element for moving the lever' and 'movable link member for holding the lever . . . and for releasing the lever' were construed as means-plus-function limitations invoking 35 USC 112, sixth paragraph since the claimed limitations were described in terms of their function not their mechanical structure.

Thus, the Examiner's holding that the word "means" is necessary for the construction of 35 USC §112 is incorrect. The current state of the law regarding the sixth paragraph is believed to be that, while the use of the word "means" provides a presumption that the sixth paragraph is intended and the absence of the word "means" is a presumption that sixth paragraph treatment was not intended, these presumptions can be rebutted.

In the present claims, the Examiner is obligated to treat the subject matter of the claims either one way or the other. If he treats the claims as not subject to the sixth paragraph of §112, he must construe the functional recitations as being included in the structure of the "address generation logic" and the "operand routing logic" because without these limitations, address generating logic and operand routing logic is meaningless. Alternatively, should the Examiner construe the address generation logic and the operand routing logic to be in means-plus-function form, then the specific structures (achieving the functions specified in the claim) are disclosed in Applicant's specification and the claim must be construed to cover those structures and equivalents thereof.

Regardless of which method the Examiner uses to construe the "address generation logic" and "operand routing logic" in independent apparatus claim 1 (as opposed to the specifically recited steps in independent method claim 22), the Examiner must construe these logical functions to include the structure for creating the claimed functional interrelationships between the processing core so as to achieve the stated results.

The Examiner quotes Applicant's statement "the claim positively recites the corresponding structure which performs the claimed functions" from Applicant's previously submitted Amendment (Remarks, page 16, third paragraph). This statement is completely correct regardless of whether the Examiner considers the claim to be limited to the structure of logic for accomplishing the specified functions or covers the corresponding structure in the specification which performs the claimed functions. In either instance, the claims positively recite structure which performs the claimed functions and therefore this is the structure which must be anticipated or rendered obvious in any cited prior art reference.

The Examiner's assessment of claim 22 as not invoking 35 USC §112 (sixth paragraph) is even more suspect. The Examiner states that "the limitations do not use the term 'step for'" language, but ignores the fact that the claims do recite "the steps of: . . . ." The ordinary English language usage of this phrase means that the method claim must be construed to include the step of receiving, the step of generating, the step of adding together, the first step of routing and the second step of routing. Furthermore, Applicant is unaware of any legal distinction between the phrase "step for" and "step of." The Examiner does not elaborate and therefore his assessment that the method steps set out in method claim 22 do not positively recite functions performed by the steps is respectfully traversed.

In paragraph 31 of the Final Rejection, the Examiner argues that "the features upon which the applicant relies . . . are not recited in the rejected claims." The Examiner does not identify where Applicant allegedly provides these arguments. However, it is seen that the paragraph bridging pages 17 and 18 in Applicant's previous Amendment draws the Examiner's attention to where the logic elements and/or means-plus-function elements are disclosed in Applicant's specification. Whichever way the Examiner construes the claim - either the logic elements having the recited functions or the corresponding means-plus-function elements – the structure or steps must be disclosed in the prior art. As noted in Applicant's previously filed response, they are not.

The Examiner also alleges that Applicant relies upon the feature of "enabl[ing] one particular shift and add operation to be performed as fast as possible." The Examiner is apparently referring to the discussion of one benefit of the present invention discussed in the first full paragraph on page 20 of Applicant's previously filed Amendment. There is no requirement

in the statute or the MPEP that a benefit of a combinations of elements must be recited in the claim. In fact, benefits of claimed inventions are generally not included in the claim language.

However, unexpected benefits resulting from claimed combinations of elements (even where those benefits are not recited in the claims) have been used by the court as evidence of non-obviousness. Applicant's previous discussion simply identifies not only the fact that the present invention improves the performance of a data processing apparatus, but also notes that none of the Applicant's Admitted Prior Art (AAPA) contains any recognition of a problem with the speed of operation of such shift and add operations, let alone any recognition of the combination of elements from three separate prior art embodiments in order to solve the problem.

Therefore, Applicant does not rely upon a feature of the claimed invention, i.e., "enable one particular shift and add operation to be performed as fast as possible," but rather a benefit of the claimed invention and therefore goes to the non-obviousness of the claims. The Examiner' statement that limitations from the specification are not read into the claims is a non sequitur, in that performing an operation as fast as possible is not a limitation from the specification, but rather, a benefit of the claimed combination of recited elements.

In section 32 of the Final Rejection, the Examiner attempts to establish a basis for picking and choosing elements from three different embodiments disclosed in Applicant's Figures 3, 4 and 5, where the impropriety of such practice was pointed out in the previously filed Amendment (see the last paragraph on page 18). However, Applicant pointed out that at no point in Figure 3 or its related discussion is there any disclosure of Applicant's claimed "operand routing logic . . . for routing operands . . . via operand manipulation logic for manipulation of said

operands prior to routing to said address generation logic." In the Amendment, Applicant invited the Examiner to identify where this disclosure is contained in any portion of Figure 3 or the discussion of Figure 3. Even though requested, the Examiner did not provide any such identification.

Similarly, as Applicant noted on page 19 (the entire page) of the previous Amendment, there is simply no reason for combining portions of Figures 3, 4 and 5, as each is a completely different way to accomplish the desirable result of address generation. Rather, the Examiner has taken bits and pieces from each of these three different ways of accomplishing the result and combined those bits and pieces in the manner disclosed only by Applicant's claim.

Regarding the Examiner's attempted defense of his hindsight reasoning of combining elements from three distinctly different embodiments (as shown in Figures 3, 4 and 5), the Examiner clearly misunderstands what is taught in Applicant's specification regarding the prior art references. The Examiner suggests in paragraph 8, page 4, that "ADD unit 170" comprises the claimed "address generation logic" of claim 1. However, ADD unit 170 of Figure 5 cannot possibly be the counterpart of the claimed address generation logic because it is not capable of "generating a shifted operand" (from Claims 1 & 22) from one of the received operands.

The Examiner contends that multiplexer 130 of the ADD unit 170 (as discussed in the Figure 4 description) performs the function of generating a shifted operand. In making this assertion, the Examiner references some unsourced "Free On-line Dictionary of Computing" definition of the word "generate." However, contrary to the Examiner's assertion, even the quoted "Dictionary" definition does not justify the Examiner's assertion. There is no indication that multiplexer 130 anticipates the features of claim 1 which recites that the address generation

logic is "for generating a shifted operand from one of said operands" where the antecedent basis for "one of said operands" is "receiving operands associated with said instruction." The Examiner apparently does not appreciate that multiplexer 130 of Figure 4 is capable of receiving a shifted operand as an input and merely outputs that shifted operand either directly or in inverted form.

No reasonable interpretation by one of ordinary skill in the art of the phrase "to generate a shifted operand" in claim 1 would cover the function of multiplexer 130 in Figure 4 (where a previously shifted value is simply received and subsequently output). Those having even rudimentary skill in the art would not interpret a function of multiplexer 130 to be that of generating a shifted operand from a received operand. The Examiner has provided no evidence or logic which would justify this unusual operational aspect of the multiplexer 130 in Figure 4.

The Examiner contends on page 5 of the Official Action that multiplexers 155 and 165 in Figure 5 are the counterparts of Applicant's claimed "operand routing logic" as set out in claim 1. He additionally contends that shifter 160 in Figure 4 is the counterpart of the "operand manipulation logic" of claim 1. However, a reading of Figure 4 and the accompanying specification discussion of Figure 4 will show that, **if** the Examiner contends the shift circuitry 135 is a counterpart to the claimed operand manipulation logic and **if** he further contends that multiplexers 130 and 137 of Figure 4 are counterparts of the operand routing logic, it follows that this precludes the shift circuitry 135 from being considered to be a counterpart of the address generation logic.

It is clear that the adder 140 in Figure 4 cannot be a counterpart of the address generation logic because it simply performs a straight-forward add operation. Adder 140 is not capable of

generating a shifted operand as required by claim 1. Similar arguments appear in the arrangement of Figure 5 of the present application and its disclosed components. Neither the prior art arrangement of Figure 4 nor the alternative prior art arrangement of Figure 5 anticipates the subject matter of claims 1 & 22.

Turning to the prior art arrangement of Figures 3A and 3B in the present specification, these previously known arrangements combine a shift and add operation as discussed. However, even if the previously known arrangement of Figures 3A and 3B is considered to be a counterpart to the claimed address generation logic, this arrangement cannot anticipate claim 1, since there is no disclosed counterpart for the "operand routing logic."

Thus, the Examiner's contentions notwithstanding, none of the prior art arrangements discussed with respect to Figures 1-5 in the present application anticipate the subject matter of claim 1. Should the Examiner have misapprehended Applicant's claimed invention, his attention is directed to Figure 6A where the add/shift circuitry 220 corresponds to the address generation logic. The shift circuitry 216 corresponds to the operand manipulation logic also in claim 1. In the known arrangement in Figure 4, the circuit element 140 performs only an add operation, whereas the circuit element 220 in Figure 6A performs a combined add and shift operation. In the invention embodiment of Figure 6A, the shift circuitry 216 can perform any arbitrary shift operation to generate a shifted operand that is logically shifted either to the left or to the right by any number of bits between 1 and 31 (see specification, page 16, lines 8-12).

By way of contrast, the combined add/shift circuitry 220 performs a predetermined logical shift left by 2 bits corresponding to the most frequently occurring shift operation (as discussed on page 16, lines 28-31). It will be appreciated by the Examiner that in alternative

arrangements, the add/shift circuitry 220 could perform a predetermined subset of the shift operations that can be performed by the general shift circuitry 216. The fact that the shift circuitry 216 provides full functionality in performing left or right shifts for any number of bits means that the time taken to process the instruction is relatively long, wherein the combined the add/shift circuitry 220 more rapidly and efficiently performs particular add and shift operations for more frequently occurring shift operations.

Therefore, notwithstanding the Examiner's arguments contained in paragraphs 32 and 33, the known arrangements shown in specification Figures 3-5 do not address the problem or suggest the solution to the problem of address generation disclosed in Figure 6A and elsewhere in Applicant's specification and recited in claims 1 and 22. Thus, claims 1 and 22, as well as claims dependent thereon, are clearly patentable over Applicant's Admitted Prior Art.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-42 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of the above claims, he is respectfully requested to contact Applicant's undersigned representative.

DIJKSTRA
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Respectfully submitted,

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